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Amendments to the Claims

1. (Original) A semiconductor device comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer; and

a phosphorous-doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.

2. (Original) The semiconductor device of claim 1, wherein the first oxide layer is a tunnel oxide layer.

3. (Original) The semiconductor device of claim 1, wherein the second oxide layer is an oxide nitride oxide layer.

4. (Original) The semiconductor device of claim 1, wherein the first polysilicon layer is a floating gate.

5. (Original) The semiconductor device of claim 1, wherein the second polysilicon layer is a wordline.

6. (Original) A semiconductor device after re-oxidation comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon layer deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a phosphorous doped oxide layer along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and

a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.

7. (Currently Amended) The device of claim 6, wherein the height is a vertical distance from the source to a bottom edge of the first polysilicon layer and the width is a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide layer.

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13. (Original) A computer system comprising:

at least one processor;

a system bus;

a flash memory device coupled to the system bus, the memory device including one or more flash memory cells comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a phosphorous doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and

a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.

14. (New) A self aligned source of a flash memory device on a substrate, the self aligned source comprising:

a horizontal layer planar to the substrate having a first doping concentration;

a vertical layer perpendicular and coupled to the horizontal layer, the vertical layer having a second doping concentration lower than said first doping concentration; and

a vertical phosphorous-doped oxide layer provided on the vertical layer, the vertical phosphorous-doped oxide layer having a third doping concentration, said self-align source having a resistance less than a self aligned source without the vertical phosphorous-doped oxide layer, thereby permitting a trench depth deeper than the self aligned source without the vertical phosphorous-doped oxide layer.

15. (New) The self aligned source of claim 14, wherein the third doping concentration and the second doping concentration produce an effective doping concentration substantially equal to the first doping concentration..

16. (New) The self aligned source of claim 14, wherein the third doping concentration is selected from a range from about 1% to about 6%.

17. (New) The self aligned source of claim 14, wherein the third doping concentration has a thickness selected from a range of about 25Å to about 500Å.

18. (New) The self aligned source of claim 14, wherein the third doping concentration and a thickness of the vertical phosphorous-doped oxide layer are selected to achieve desired characteristics of the flash memory cell, such as program rate, ease rate, and data retention.

19. (New) A semiconductor device comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon deposited over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer; and

a phosphorous-doped oxide along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.

20. (New) A semiconductor device after re-oxidation comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon layer deposited over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a phosphorous doped oxide layer along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer; and a re-oxidation oxide profile having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide layer.